Noise Filtering Edge Detectors

BACKGROUND OF THE INVENTION

1. Field of the Invention

The previous art represented by the application PCT/CA03/000909 describes the DSP MSP invention which includes noise filters for digital filtering of a captured waveform shown in the Sec.2 of the SUMMARY OF THE INVENTION and the Sec.3 of the DESCRIPTION OF THE PREFERRED EMBODIMENT.
This invention defines much more efficient noise filters, and represents significant development of circuits and methods described in the previous art application PCT/CA03/000909.

This invention defines digital means for programmable noise filtering from over-sampled wave-forms consisting of variable lengths pulses having frequencies ranging from zero to 1/2 of technology's maximum clock frequency.

The noise filtering edge detectors (NFED) are directed to signal and data recovery in wireless, optical , or wireline transmission systems and measurement systems.

The noise filtering edge detectors (NFED) shall be particularly advantageous in system on chip (SOC) implementations of signal processing systems.

2. Background Art

The D1 (PCT/CA03/000909 by Bogdan) allocates generic processing stages for noise filtering while designating close control and significant parts of noise filtering functions to be performed by a Programmable Control Unit (PCU).
However the present invention provides definitions of much more efficient noise filtering functions and specifies more efficient hardware means for said functions implementation than that enabled by D1.
Therefore the present invention defines algorithms and processing stages enabling faster and much more efficient noise filtering functions than those enabled by the D1 requiring more supervision and more involvement of said more universal but slower PCU.
Consequently this invention allows processing of signals having SNR significantly lower than that necessary for D1 error free operations.

The D2 (US 5,668,830 by Georgiou at al) is limited to using delay lines and basic re-timing of a front edge for removing phase sample noise.
D2 circuits enable merely phase aligning and data re-timing on a bit per bit basis for data serializing/de-serializing only, while being unable to eliminate narrow glitches from inside of NRZ streams of data bits.

D2 does not have any of the fundamental features of the present invention such as; continuity of over-sampling of entire pulse necessary for amplitude glitches elimination, or high processing throughput necessary for calculating and processing of discrete time noise filtering integrals, or wave-form screening and adaptive noise filtering.
D2 can not be as effective in noisy environments as the presented invention, since it requires SNR by several times higher than that acceptable for the presented invention.

SUMMARY OF THE INVENTION

The NFED invention provides an implementation of programmable algorithms for noise filtering for a very wide range of low and high frequency wave-forms.

The NFED comprises; use of a synchronous sequential processor (SSP) for real time capturing and processing of in-coming wave-form, and use of a programmable computing unit (PCU) for controlling SSP operations and supporting adaptive noise filtering and edge detection algorithms. (see also the Sec.2 of the SUMMARY OF THE INVENTION in the PCT/CA03/000909).

The NFED comprises using a set of binary values as an edge mask which is compared with a set of captured binary values surrounding a bit of a captured waveform buffer, in order to check if the captured bit represents an edge of the waveform.
Said comparison comprises:
- performing logical and/or arithmetic operations on particular bits of the edge mask and their counterparts from the waveform samples surrounding the particular bit of the waveform buffer;
- Performing arithmetic and/or logical operations on the results of said operations, in order to estimate waveform's edge proximity figure (EPF);
- Comparing the EPF with an edge threshold, in order to determine if the captured bit represents an edge of the waveform.

The NFED further comprises modulating placement of detected rising and/or falling waveform edges by an edge modulating factor (EMF) calculated as a function of the EPF, were said function is controlled by an edge modulation control register (EMCR) which is preset by an external control unit.

The NFED still further comprises displacing detected rising and/or falling waveform edges by a preset number of bits, in order to compensate for ISI's and/or other duty cycle distortions.

The NFED invention further includes:
- using the WFSC for incoming waveform registration and monitoring (see also the Sec.2 of the SUMMARY OF THE INVENTION in the PCT/CA03/000909);
- programmable waveform analysis and adaptive noise filtering algorithms;
- edge mask registers for providing said edge masks used for detecting rising and/or

falling waveform edges;

- edge threshold registers for providing said edge thresholds used for detecting rising and/or falling waveform edges;
- edge displacement registers for providing said edge displacement numbers used for shifting detected rising and/or falling edges by a programmable number of bits of waveform processing registers;
- filter control registers which control; said logical and/or arithmetic operations conducting the comparison of captured waveform bits with the edge mask, and said edge displacements in the processed waveforms;
- using the PCU for calculating and loading said edge mask registers and/or said edge threshold registers and/or said edge displacement registers and/or said filter control registers;
- using the PCU for controlling said calculations of the EMF by presetting the EMCR in accordance with adaptive noise filtering algorithms.
- using the PCU for controlling and using the WFSC operations for implementing adaptive filters by controlling noise filtering edge detection stages of the SSP.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The preferred embodiment implements the above defined general components of the NFED and is shown in FIG.5, FIG.6 and FIG.7.

Said NFED comprises the multi-sampled phase (MSP) capturing of incoming wave-form intervals in specifically dedicated wave interval registers which are further rewritten to wave interval buffers (see the FIG.5 showing the wave registers 1WR,2WR followed by the wave buffers 11WB, 12WB, 21WB, 22WB).

In order to provide all wave samples needed for the filtering edge detection along a whole wave buffer, the NFED invention includes rewriting:

- the end part 2WR(R:(R-M+1) of the wave register 2WR, into the front parts 11WB(M:1),12WB(M:1) of the wave buffers 11WB,12WB;
- the end part 1WR(R:(R-M+1) of the wave register 1WR, into the front parts 21WB(M:1),22WB(M:1) of the wave buffers 21WB,22WB.

The preferred embodiment is based on the assumptions listed below:

- the wave registers 1WR and the 2WR are 15bit registers (i.e. R=14);
- the rising edge mask REM(M:0) and the falling edge mask FEM(M:0) are 8bit registers (i.e. M=7) and the PCU loads the same masks equal to 00001111 to both mask registers;
- the rising edge threshold RET is loaded with 0110 (6 decimal), and the falling edge threshold FET is loaded with 0010 (2 decimal);

The digital filter arithmometers 21DFA1/22DFA1/11DFA1/12DFA1 perform all the comparison functions, between the edge mask registers REM/FEM and the waveform buffers 21WB/22WB/11WB/12WB involving the edge threshold registers RET/FET, with the 3 basic operations which are further explained below.

The first operation is performed on all the waveform bits and involves the edge mask bits as it is specified below:

For every waveform's consecutive bit WB_k the surrounding bits WB_{k-4}, WB_{k-3}, WB_{k-2}, WB_{k-1}, WB_k, WB_{k+1}, WB_{k+2}, WB_{k+3} are logically compared with the mask bits B_0, B_1, B_2, B_3, B_4, B_5, B_6, B_M and the resulting 8bit binary expression $BE_k(7:0)$is created as equal to;
$BE_k(0) = (WB_{k-4}=B_0)$, $BE_k(1) = (WB_{k-3}=B_1)$, $BE_k(2) = (WB_{k-2}=B_2)$,
$BE_k(3) = (WB_{k-1}=B_3)$, $BE_k(4) = (WB_k=B_4)$, $BE_k(5) = (WB_{k+1}=B_5)$,
$BE_k(6) = (WB_{k+2}=B_6)$, $BE_k(7) = (WB_{k+3}=B_7)$.
The second operation adds arithmetically all the bits of the binary expression $BE_k(7:0)$ and the resulting edge proximity figure EPF_k is calculated as equal to $EPF_k= BE_k(0) + BE_k(1) + BE_k(2) + BE_k(3) + BE_k(4) + BE_k(5) + BE_k(6) + BE_k(7)$ which shall amount to a 0 - 8 decimal number.
The third operation performs functions explained below:

- The verification is made if the EPF_k indicates a rising edge condition by exceeding the content of the rising edge threshold RET(T:0). Consequent detection of the $EPF_k > RET = 6$ condition, sets to level = 1 the corresponding $DFR1_k$ bit of the DFR1 and all the remaining bits of the present DFR1 until a falling edge is detected as it explained below.
- The verification is made if the EPF_k indicates a falling edge condition by being smaller than the content of the falling edge threshold FET(T:0). Consequent detection of the $EPF_k < RET = 2$ condition, sets to level = 0 the corresponding $DFR1_k$ bit of the DFR1 and all the remaining bits of the present DFR1 unless a rising edge is detected as it explained above.

In order to carry the same level from the last bit of the previous phase DFR1 into the following bits of the present phase digital filter register2 (DFR2), the last bit DFR1(R) of the previous DFR1 is rewritten into the carry bit DFR1(C) of the present DFR1 and is used by the digital filter arithmometer2 (DFRA2) to fill front bits of the DFR2 with the same level as the last bit of the previous phase DFR1.

The digital filter arithmometers 21DFA2/22DFA2/11DFA2/12DFA2 perform; the inter-phase continuation of filling front bits of the present phase register in accordance with the level set in the last bit of the previous phase, followed by said edge displacement which compensates for duty cycle distortions due to ISIs, etc..
The edge displacement comprises the 3 basic operations described below.

- Any DFR1 rising edge, indicated by a level 0 to 1 transition, is shifted left by a number of bits specified by a content of the rising edge displacement register (RED(D:0)) loaded by the PCU in accordance with its filtering algorithms.
- Any DFR1 falling edge, indicated by a level 1 to 0 transition, is shifted left by a number of bits specified by a content of the falling edge displacement register (FED(D:0)) loaded by the PCU in accordance with its filtering algorithms.
- In order to propagate said displacement operations from the present phase to the previous phase; the propagated sign of the edge bit (DFR2(Sp)) and the propagated bits (DFR2(Dp:0)), are calculated by the DFA2 and are written down into the DFR2 extension DFR2(Sp,Dp:0).

In order to propagate said displacement operations from the next phase DFR2 into end bits of the present phase digital filter register3 (DFR3); the propagated sign of the edge bit and the propagated displaced bits DFR2(Sp,Dp:0) from the next phase, are used by the digital filter arithmometer3 (DFRA3) to fill end bits of the digital filter register3 (DFR3) with the

correctly displaced bits propagated form the next phase to the present phase.

As it is shown in the FIG.5, FIG.6, FIG.7; all the timing and circuits for any further waveform processing can remain similar as shown in the PCT/CA03/000909 application with the differences based on increasing clock numbers by 3 starting from the Clk2; i.e. the 1Clk2 shall be replaced by the 1Clk5, and so on.